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FIG. 1

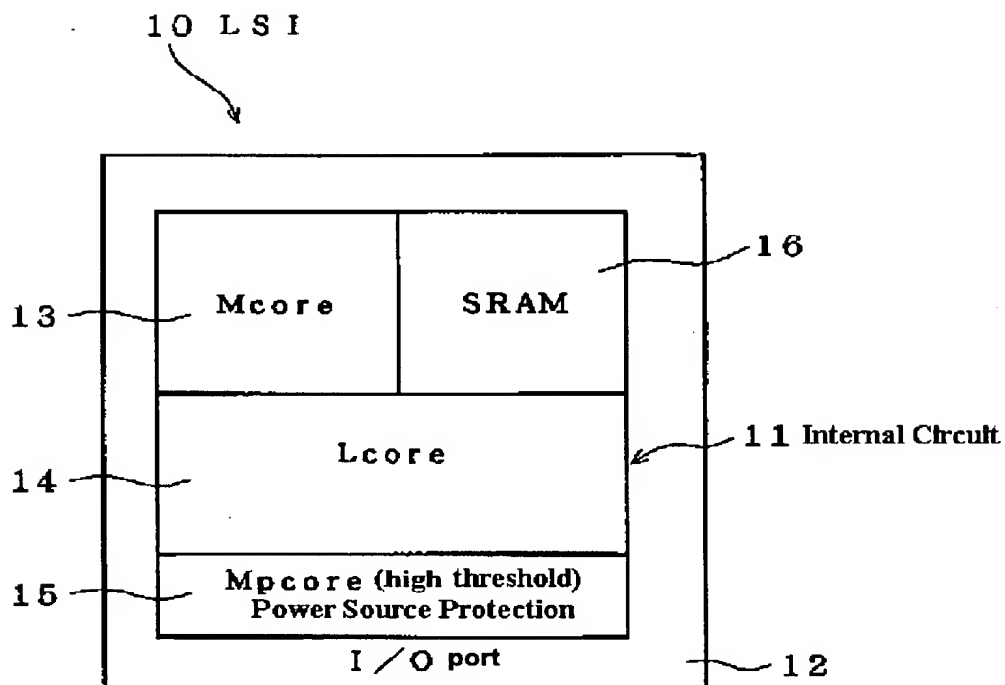
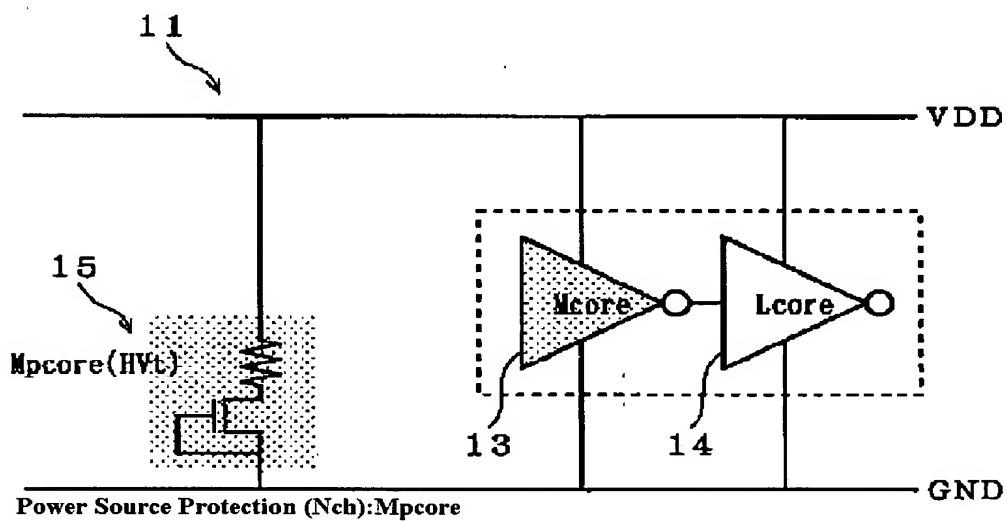


FIG. 2



Title: SEMICONDUCTOR DEVICE
AND MANUFACTURING
METHOD THEREOF

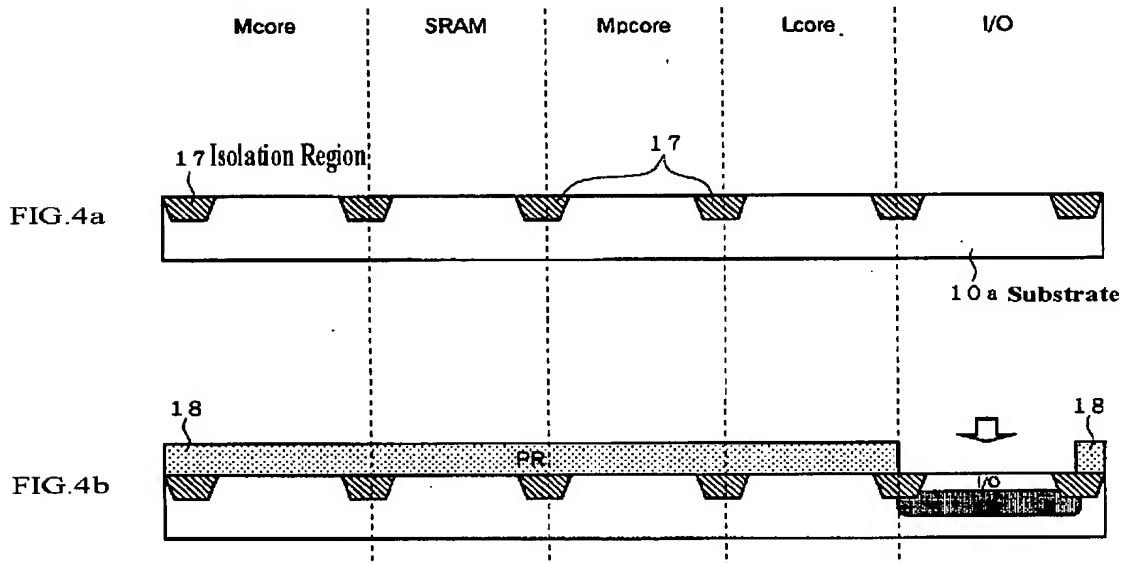
Inventor(s): Naoto AKIYAMA

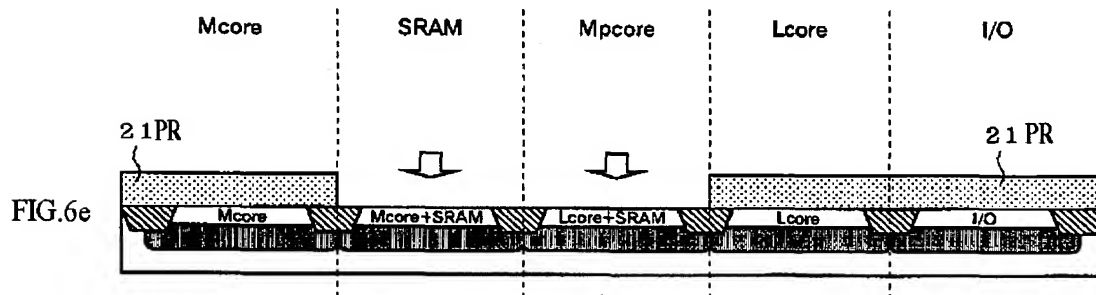
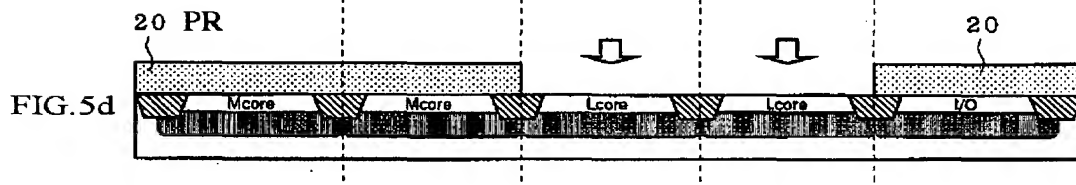
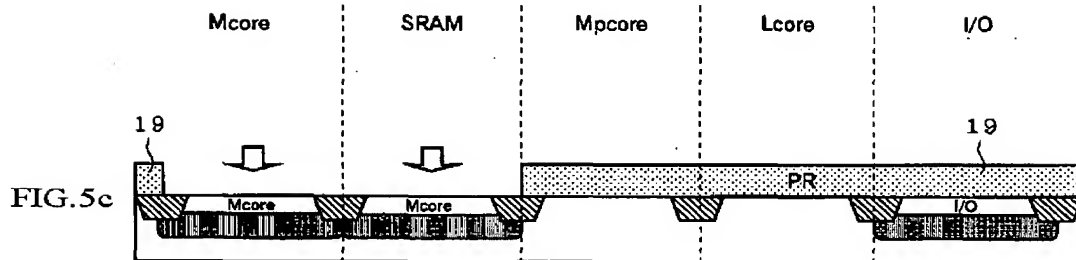
Atty. Dkt. No. 029437-0102

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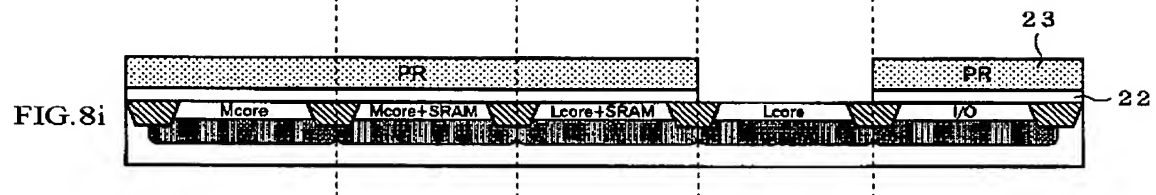
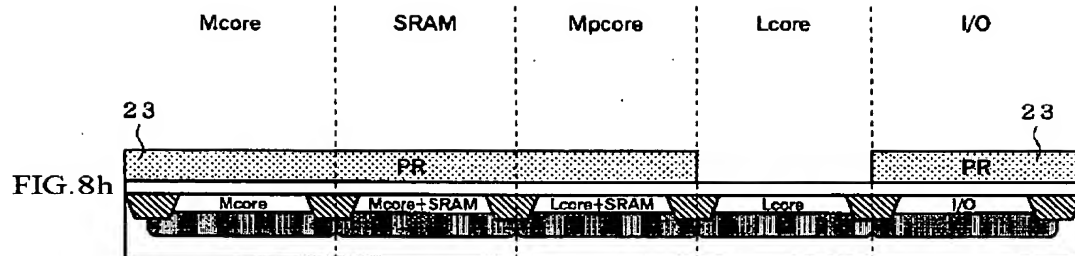
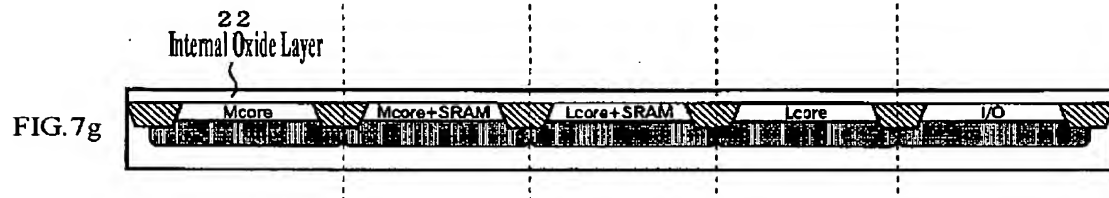
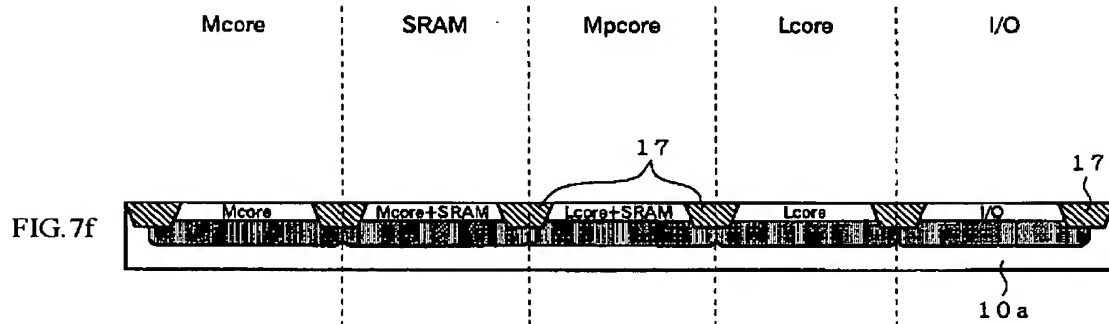
FIG. 3

	Internal Circuit		Power Source Protector	I/O (External Interface)
	Mcore	Lcore	Mpcore(EVt-M)	
thickness of gate dielectric layer (nm)	1.9	2.6	1.9	(7.2)
operating voltage (V)	1.2	1.2	1.2	(3.3)
threshold voltage V_t	low	high	higher than Mcore	
leak/off current	large	small	smaller than Mcore	
speed	high	low		
power consumption	large	small		
breakdown voltage of gate dielectric layer	low(about 5V)	high (about 7V)	same as Mcore	(high, about 10V)





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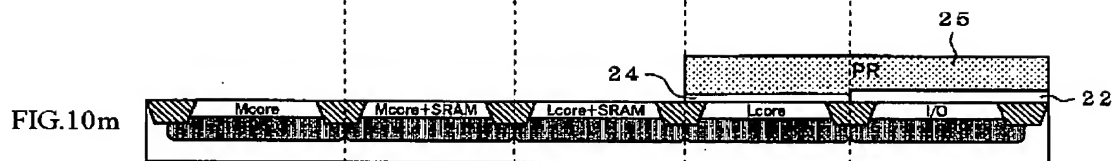
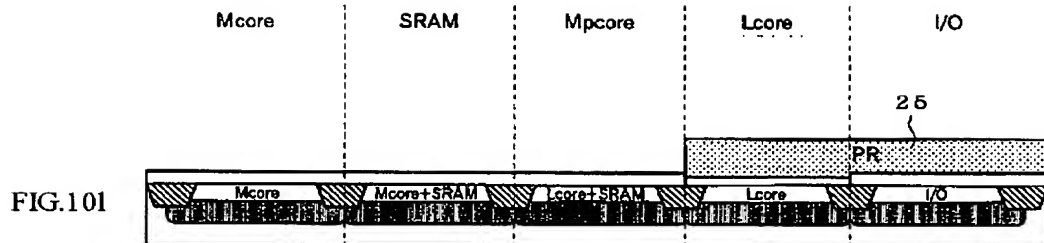
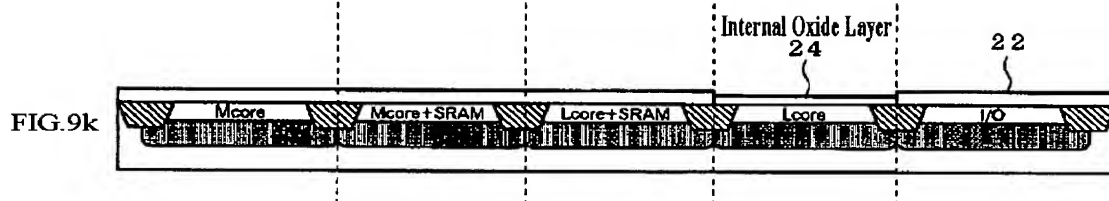
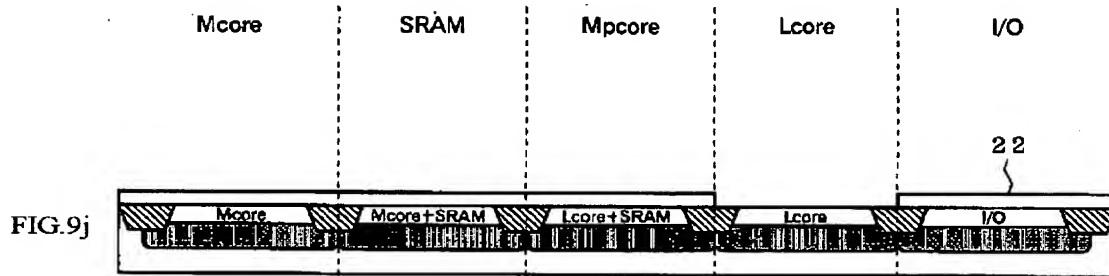


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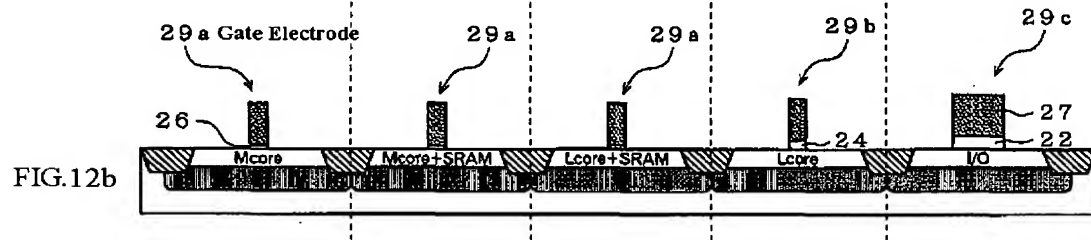
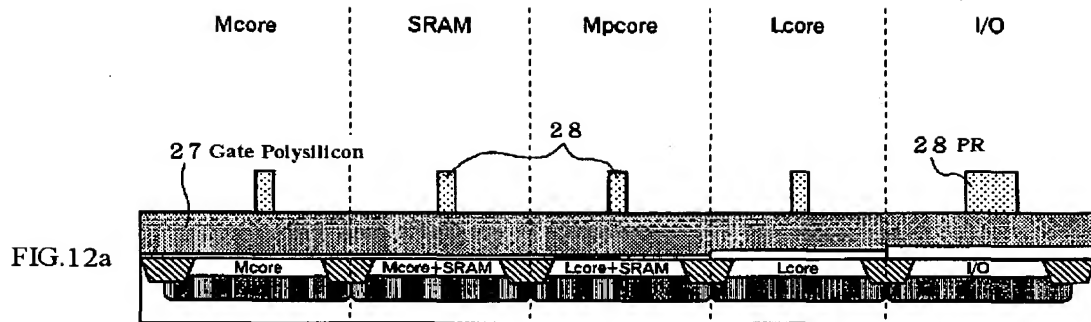
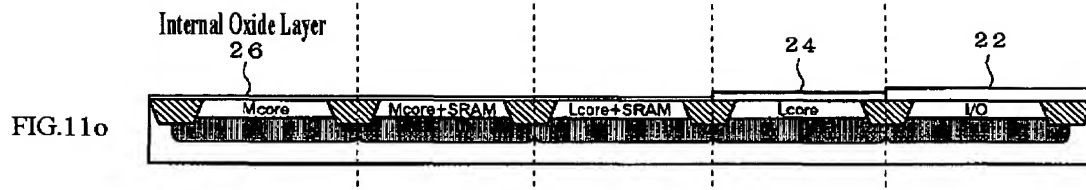
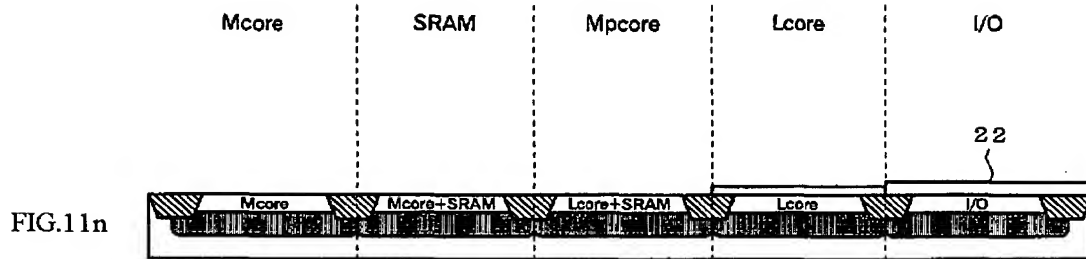
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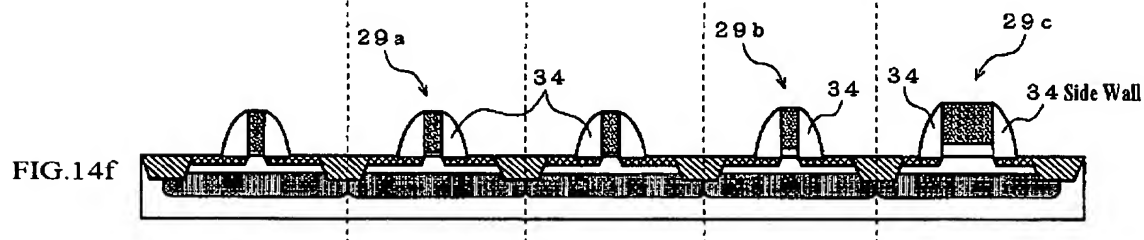
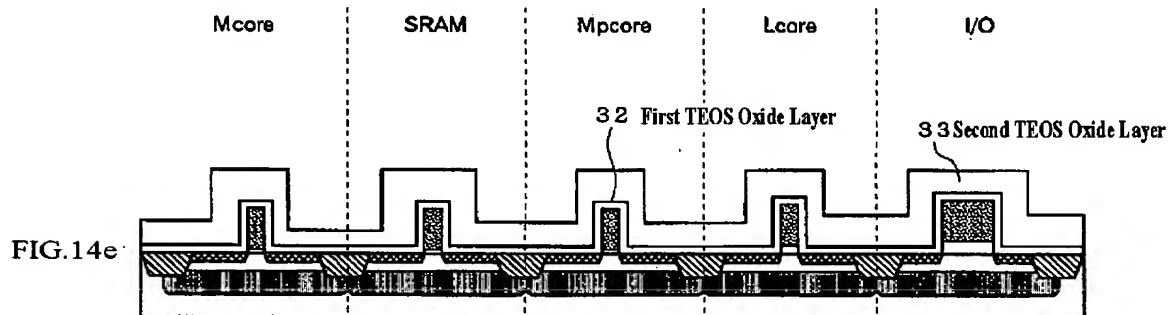
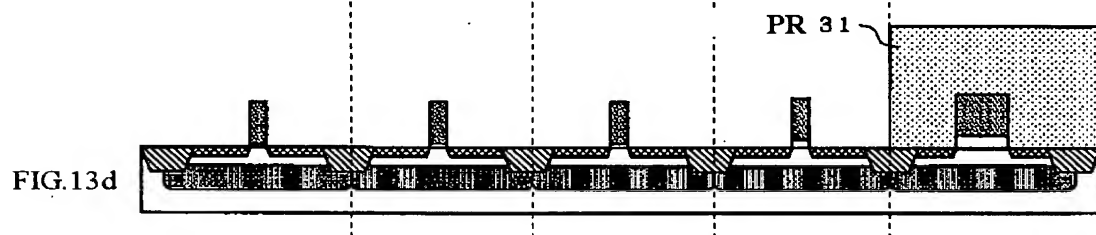
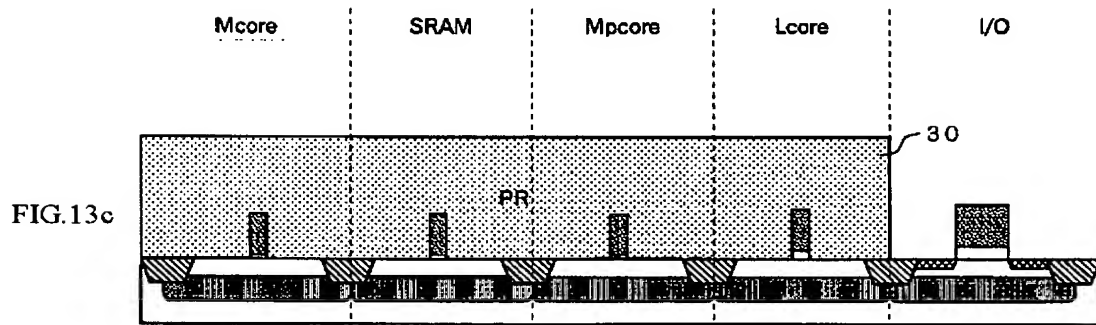


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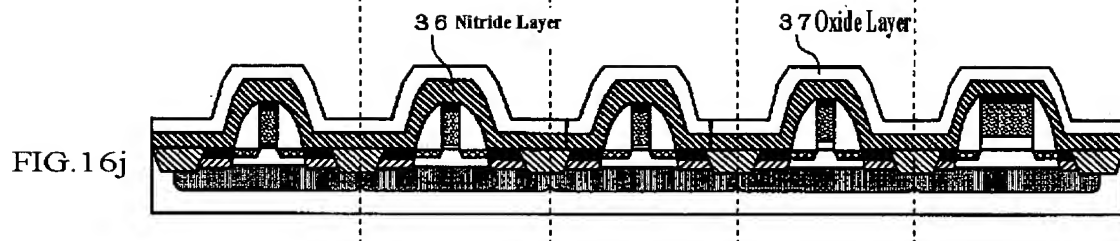
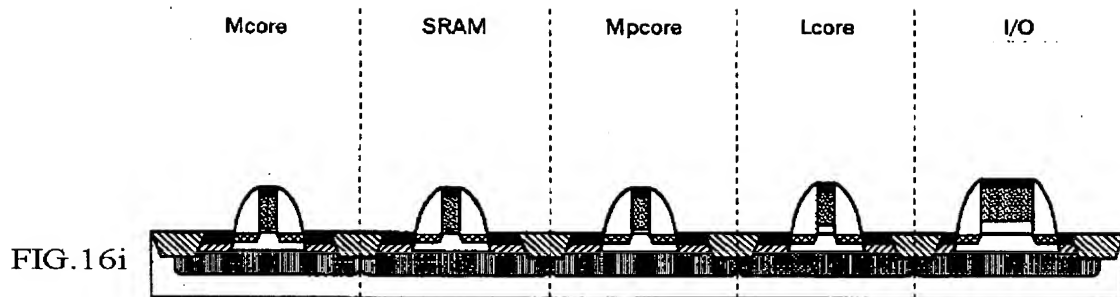
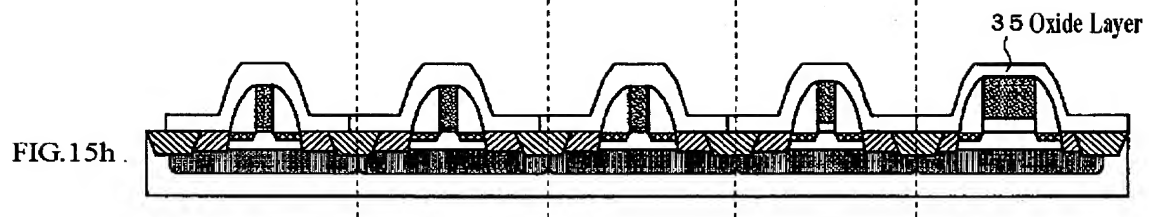
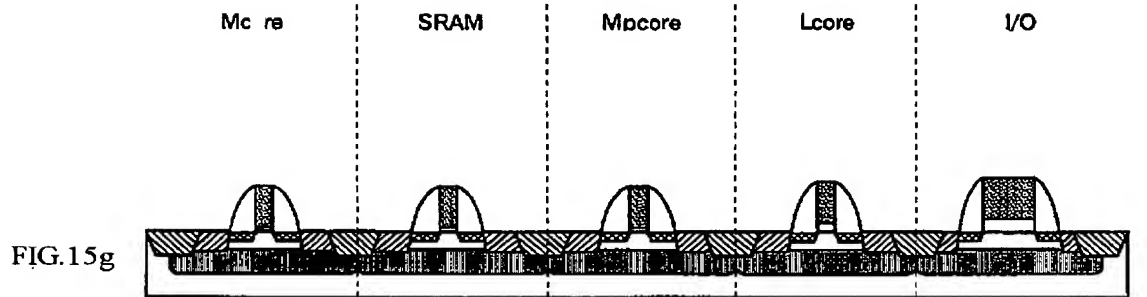


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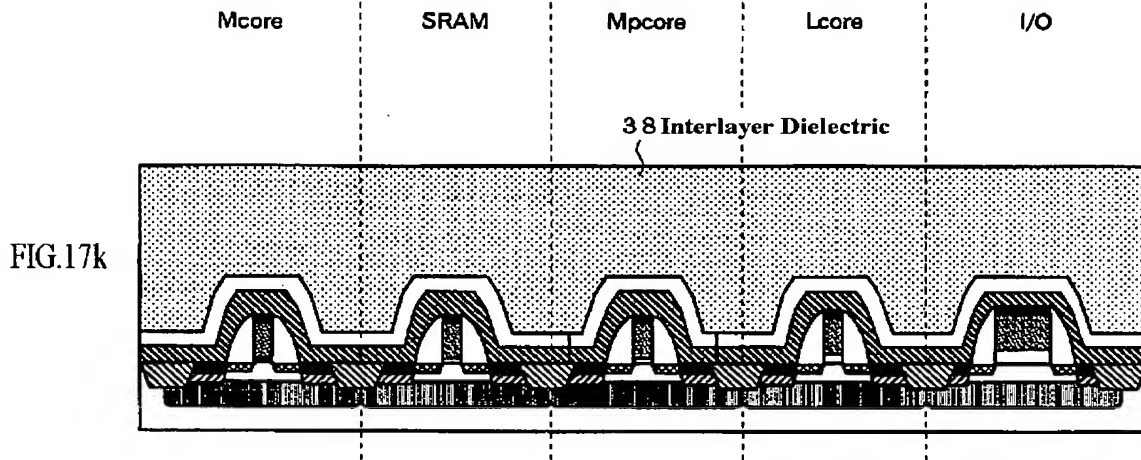


FIG. 18

